Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 7002

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – MAY / JUNE 2024
Eighth Semester
Electronics and Communication Engineering
U19ECE19 – SYSTEM-ON-CHIP DESIGN
(Regulation 2019)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q. No.	Questions	Marks	KL	CO
1.	What are the advantages and disadvantages of driving forces for SoC?	2	K1	CO1
2.	Mention hardware-software partitioning in SoC.	2	K2	CO1
3.	What is the purpose of address and data lines related to bus terminology?	2	K2	CO2
4.	What is VLIW architecture?	2	K2	CO2
5.	How the buffer is designed for a fixed or maximum request rate?	2	K1	CO3
6.	Define Interconnection.	2	K1	CO3
7.	What is meant by reconfiguration?	2	K2	CO4
8.	Enumerate ARM classification.	2	K2	CO4
9.	Write a Verilog module for Multipliers.	2	K2	CO5
10.	Mention the features of VHDL.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q. No.		Questions	Marks	KL	CO
11.	a)	What is the difference between the spiral model and the waterfall model? What is specification-based design? Explain.	13	K2	CO1
		(OR)			
	b)	Mention & explain the SoC design, test, layout, and characteristics.	13	K2	CO1
12.	a)	Differentiate between CISC and RISC. What is Cache memory? How is MMU different from the main memory?	13	K2	CO2
		(OR)			
	b)	Differentiate between concurrent statement (combinational) and procedural statement (sequential) in Verilog using suitable examples. Write a Verilog module for the full adder.	13	K2	CO2
13.	a)	Draw and explain ARM-based system-on-chip architecture with detailed functionality.	13	K1	CO3
		(OR)			
	b)	Explain the basic bus physical structure, with a diagram.	13	K2	CO3
14.	a)	Differentiate between non-pipelined and pipelined bus data transfer modes with neat waveforms.	13	K3	CO4
		(OR)			
	b)	Discuss how custom Instructions are automatically identified.	13	K3	CO4
15.	a)	How is verification performed using simulation in Verilog? Explain synthesis and device implementation on an FPGA development board using Verilog HDL.	13	K4	CO5
		(OR)			
	b)	How is the effectiveness of a customization to be estimated? Explain.	13	K4	CO5

PART – C

(1 x 15 = 15 Marks)

Q. No.			Questions	Marks	KL	CO
16.	a)	i.	Explain PLDs and provide their classification.	7 + 8	K3	CO2
		ii.	Discuss the tools and techniques for designing, verifying, and implementing SoC using programmable logic.			
			(OR)			
	b)		Concerning the application study, explain the 3-D Graphics Processors, with examples & diagrams.	15	K4	CO5